

100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195

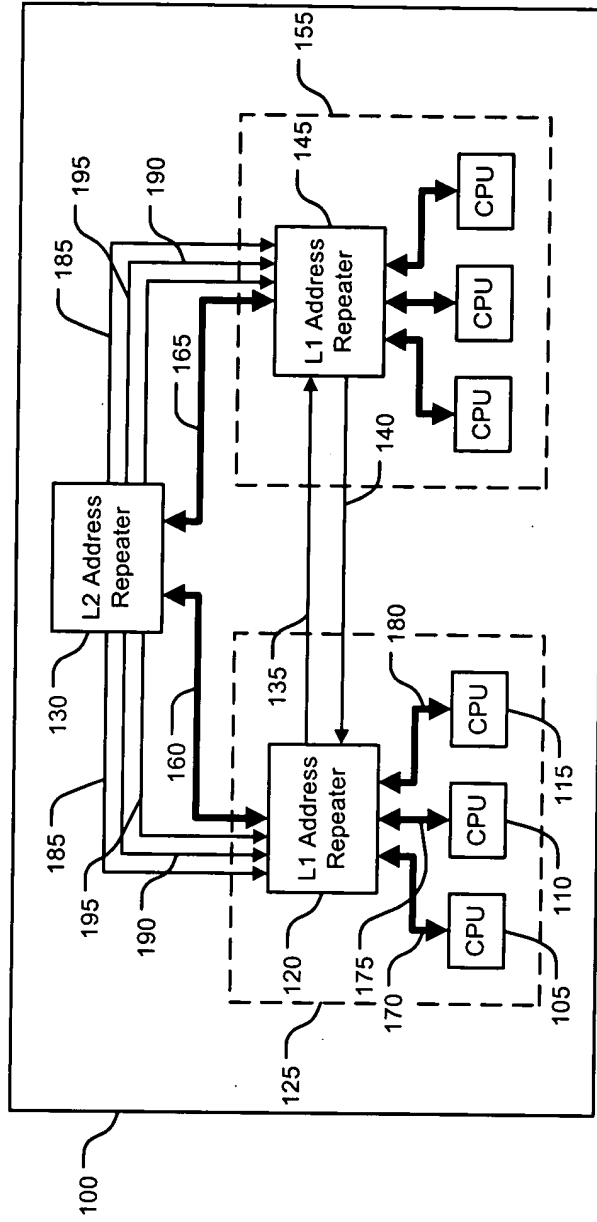


Figure 1

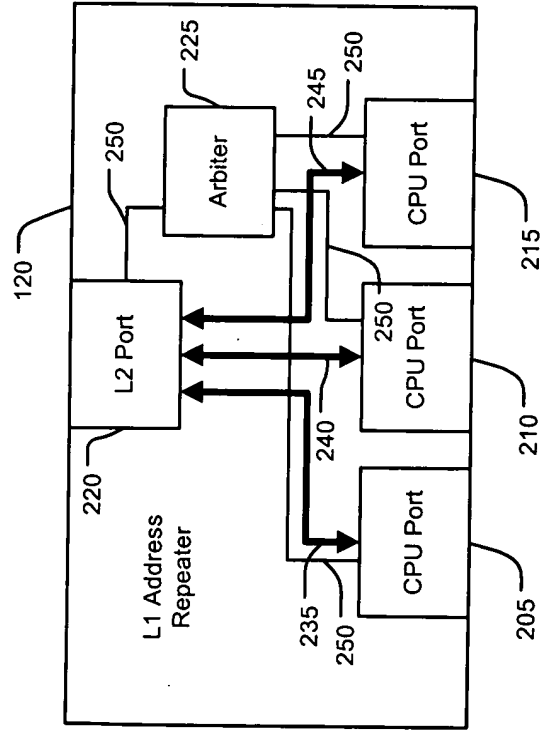


Figure 2

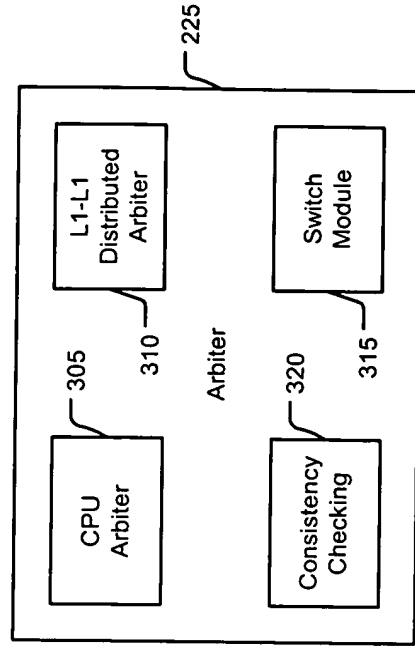


Figure 3

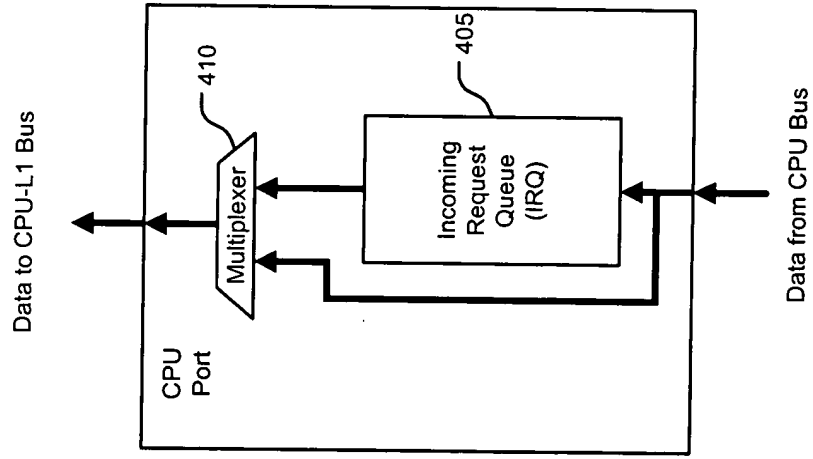


Figure 4(a)

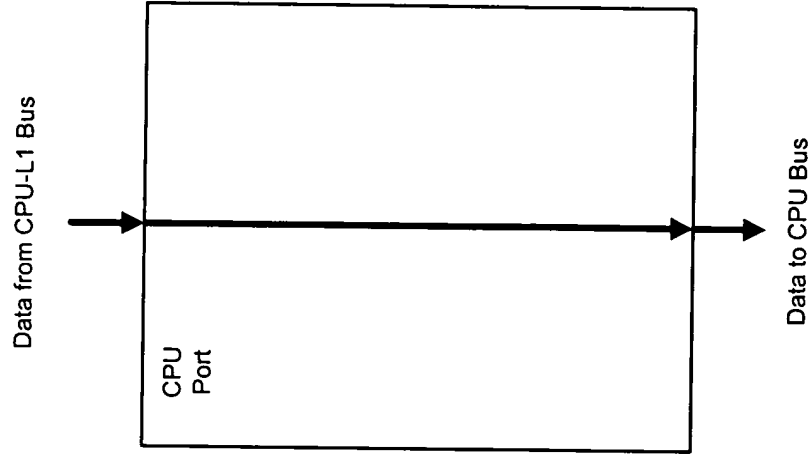


Figure 4(b)

Figure 5 is a block diagram of an L2 Port. The L2 Port is connected to an L2 Address Repeater. The L2 Port includes an Input Multiplexer (505) and an Outgoing Request Queue (ORQ) (510). The Input Multiplexer (505) receives data from CPU-L1 Bus 235, CPU-L1 Bus 240, and CPU-L1 Bus 245. The Input Multiplexer (505) outputs data to the L2 Address Repeater. The Outgoing Request Queue (ORQ) (510) receives data from the L2 Address Repeater and outputs data to the ORQ Multiplexer / Output Demultiplexer (515). The ORQ Multiplexer / Output Demultiplexer (515) outputs data to CPU-L1 Bus 235, CPU-L1 Bus 240, and CPU-L1 Bus 245.

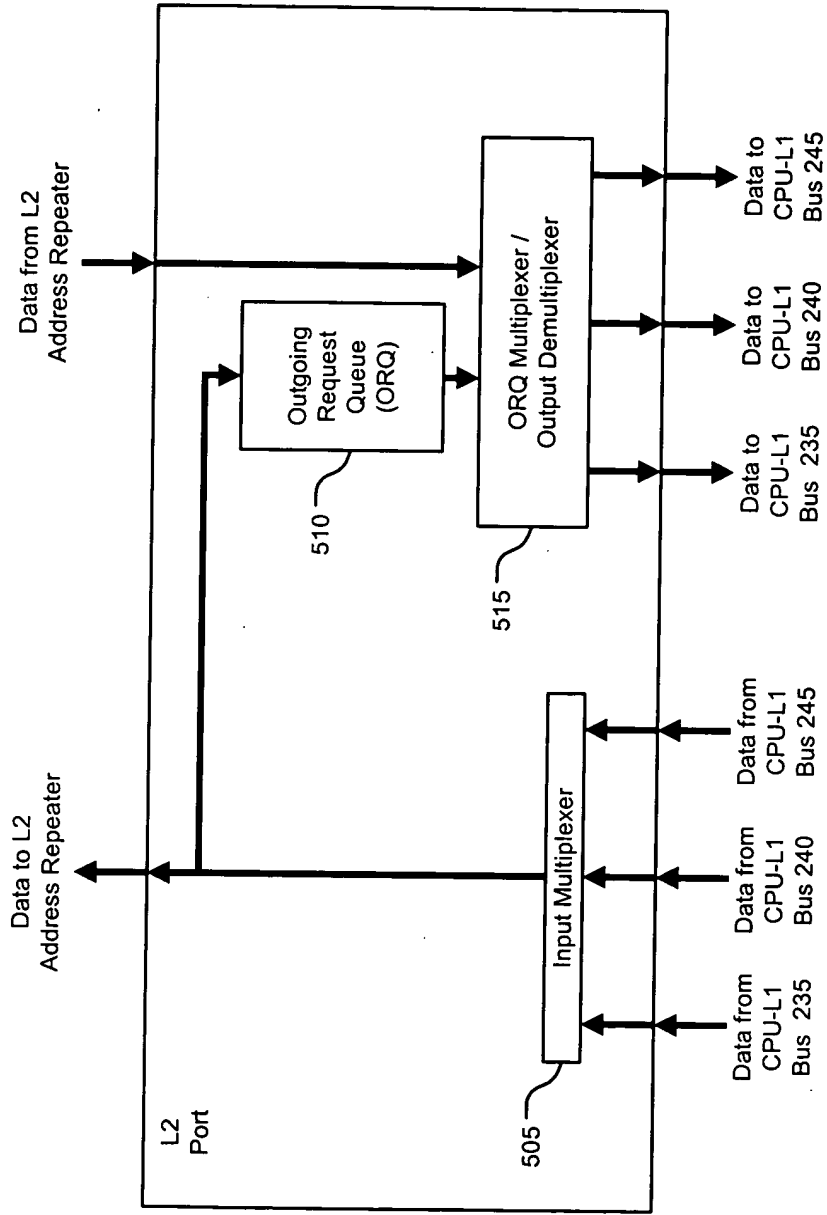


Figure 5

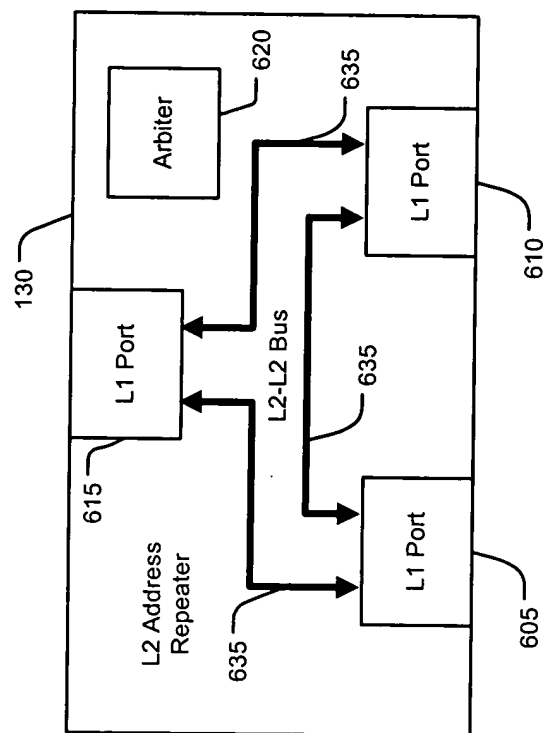


Figure 6

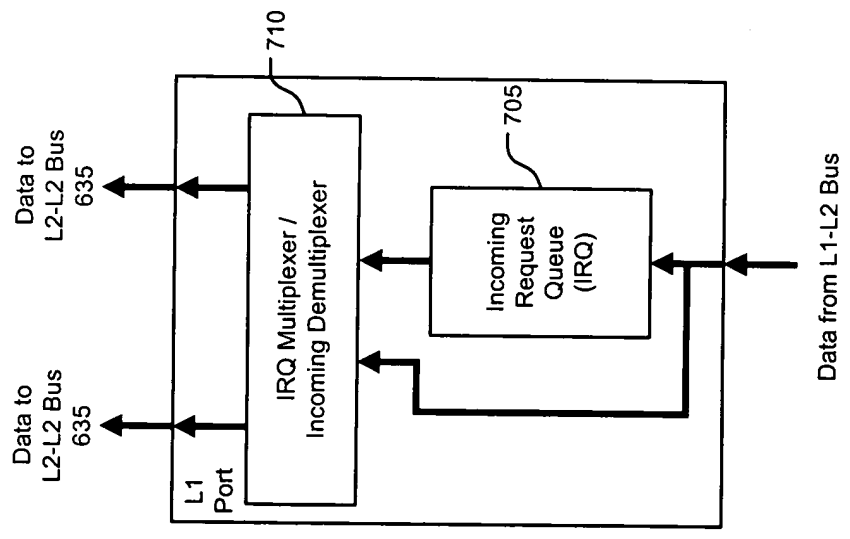


Figure 7(a)

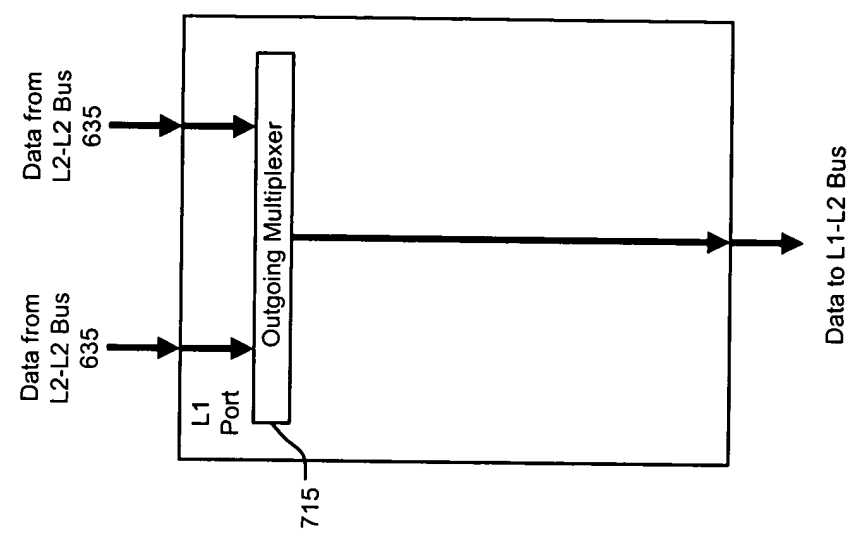


Figure 7(b)

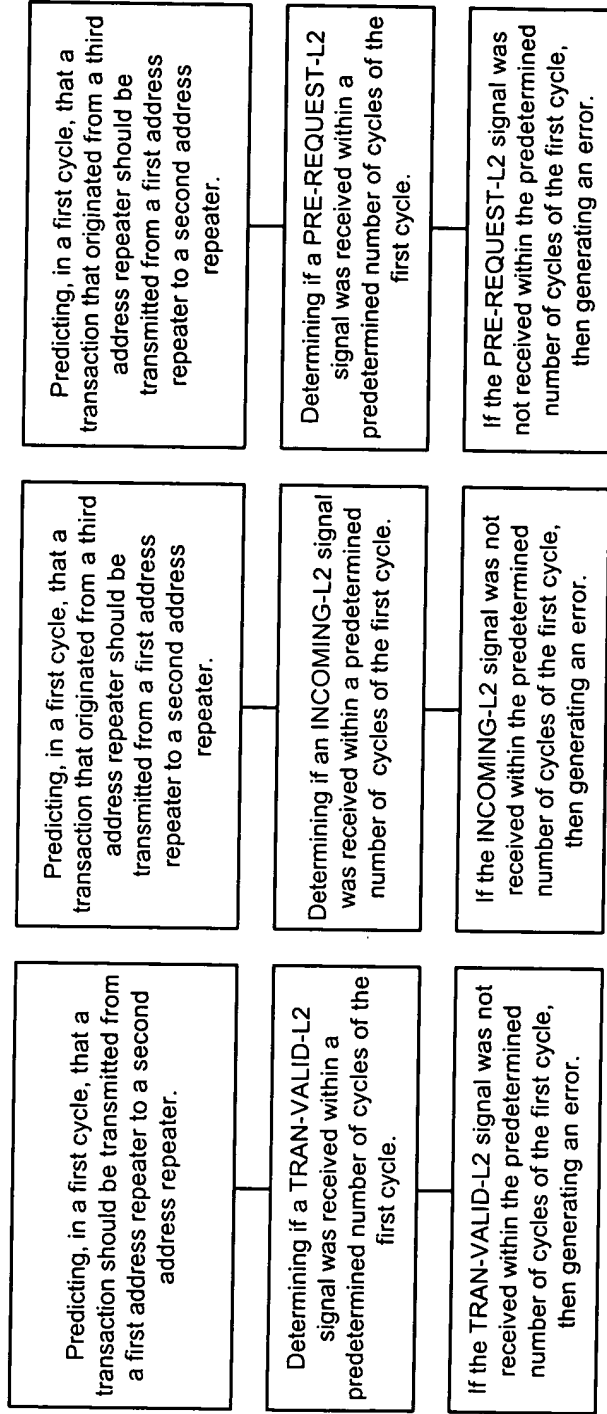


Figure 8(a)

Figure 8(b)

Figure 8(c)

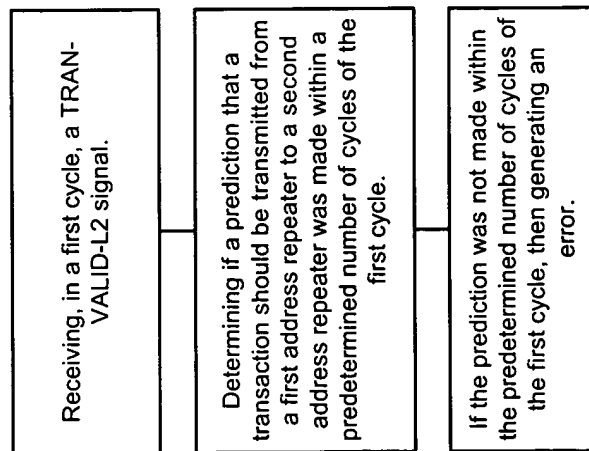


Figure 9(a)

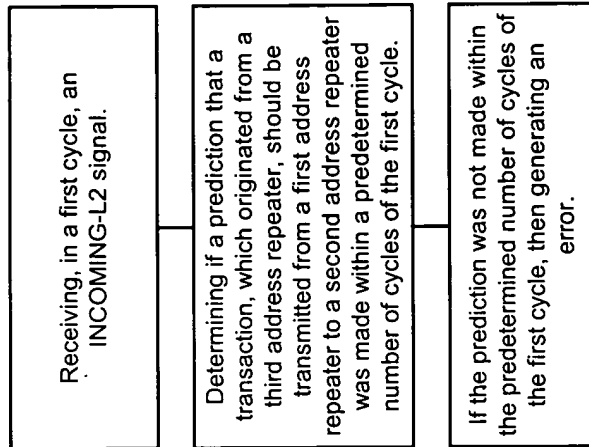


Figure 9(b)

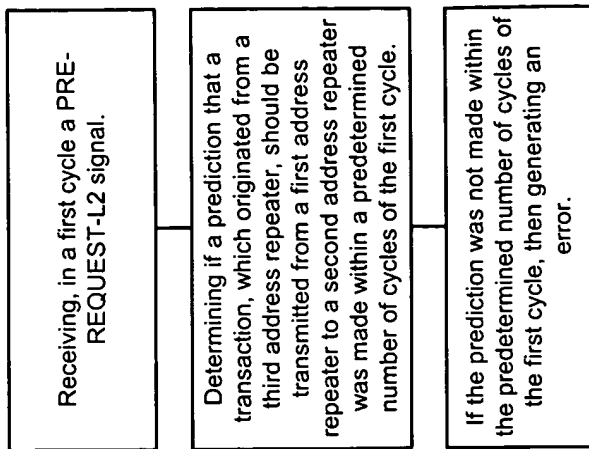


Figure 9(c)